Synthesized Clock Generator

CG635 — 0.001 Hz to 2.05 GHz low-jitter clock generator

CG635 Synthesized Clock Generator

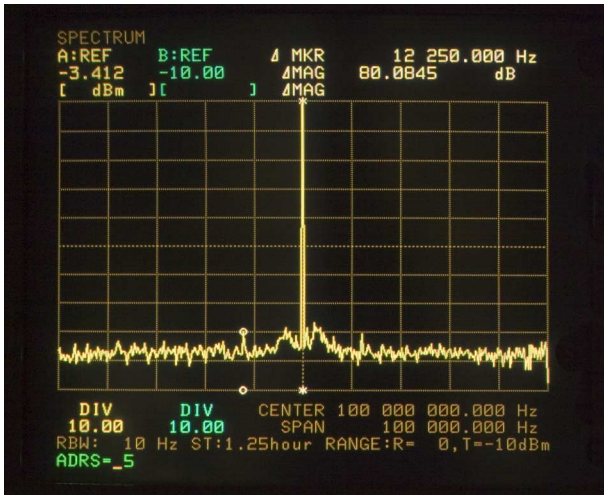
- **Clocks from 0.001 Hz to 2.05 GHz**
- **<1 ps rms jitter**
- **CMOS, PECL, ECL, LVDS, RS-485 outputs**
- **Single-ended and differential outputs**
- **Adjustable phase and time modulation**
- **PRBS for eye-pattern testing (opt.)**
- **OCXO and rubidium timebase (opt.)**

The CG635 Synthesized Clock Generator provides precise, low-jitter digital clock signals for applications ranging from the development of digital circuits to the testing of communications networks.

The CG635 generates single-ended and differential clocks from 1 mHz to 2.05 GHz with sub-picosecond jitter. Clock frequencies may be set with 0.001 Hz resolution. Front-panel outputs have continuously adjustable offsets and amplitudes, and may also be set to standard logic levels including CMOS, PECL, ECL and LVDS. A rear-panel output delivers clocks at RS-485 and LVDS levels over twisted pairs.

An optional pseudo-random binary sequence (PRBS) generator (Opt. 01) provides clock and data outputs at LVDS levels for testing serial data channels. Edge transition times are typically 80 ps.

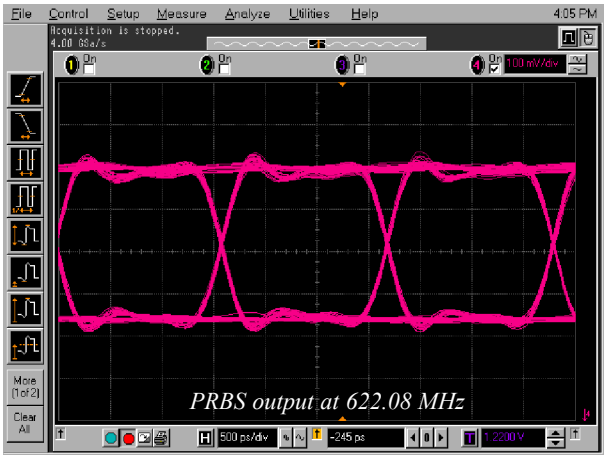
The standard crystal oscillator timebase of the CG635 provides sufficient accuracy for many applications. An optional ovenized crystal oscillator (Opt. 02), or rubidium frequency standard (Opt. 03), may be added to improve frequency stability and reduce aging. The CG635 can also be locked to an external 10 MHz timebase.



CG635 spectrum exhibiting −80 dB spurious signals

The CG635 delivers a low spurious output signal—better than most commercial synthesizers. Phase noise for a 622.08 MHz carrier at 100 Hz offset is less than −80 dBc/Hz, and the spurious response is better than −70 dBc. The frequency accuracy and drift are limited only by the reference timebase.

When compared to a typical RF synthesizer, the CG635 has many similarities—high frequency resolution, low phase noise, and low spurious output levels. It also offers several advantages—frequencies down to 1 mHz, multiple square wave outputs to 2.05 GHz, and it is much less expensive.

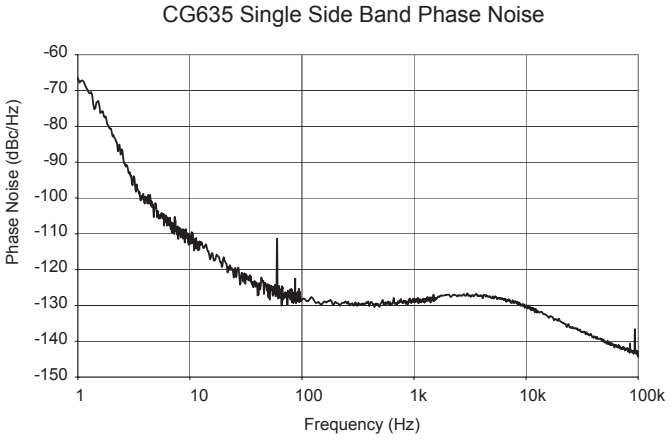


PRBS outputs are available for eye-pattern testing

Several instrument features support more complex tasks. For example, the phase of the outputs may be adjusted with 0.001° resolution, and the timing of clock edges may be modulated over ±5 ns by an external analog signal. Optional PRBS outputs are available on rear-panel SMA jacks for eye-pattern testing of serial data links.

All instrument functions may be controlled from the front panel or via the GPIB (IEEE-488.2) or RS-232 interfaces. Up to ten complete instrument configurations can be stored in non-volatile memory and recalled at any time. A universal input AC power supply allows world-wide operation.

Several clock receiver modules are available which may be connected to the rear-panel RS-485/LVDS output via Category-6 cable. These accessories provide complementary high-speed transitions at standard logic levels on SMA connectors, and may be located at a substantial distance from the instrument. CMOS (+5 V, +3.3 V and +2.5 V), PECL (+5 V, +3.3 V and 2.5 V), RF (+7 dBm), CML/NIM, ECL, and LVDS outputs are all available.



Phase noise measured at an output frequency of 10 MHz. Add +6 dB/octave above 10 MHz.

Model	Description
CG640	CMOS (+5 Vcc) to 50 MHz
CG641	CMOS (+3.3 Vcc) to 250 MHz
CG642	CMOS (+2.5 Vcc) to 250 MHz
CG643	PECL (+5 Vcc) to 1500 MHz
CG644	PECL (+3.3 Vcc) to 1500 MHz
CG645	PECL (+2.5 Vcc) to 1500 MHz
CG646	RF (+7 dBm) to 1500 MHz
CG647	CML/NIM to 1500 MHz
CG648	ECL to 1500 MHz
CG649	LVDS to 2050 MHz

Optional clock receivers for the CG635

Rear Panel Features

- Differential outputs (RS-485, LVDS)
- PRBS and clock outputs (Opt. 01)
- 10 MHz reference input
- 10 MHz output
- +5 V and –5 V accessory power
- GPIB and RS-232 interfaces
- Phase and time modulation input
- Universal input AC power supply

CG635 rear panel (with opt. 01)

Frequency

Range	0.001 Hz to 2.05 GHz
Resolution	0.001 Hz
Accuracy	$\Delta f < \pm(5\times10^{-19} + \text{timebase error}) \times f$ (1 MHz ≤ f ≤ 2.05 GHz)
	$\Delta f < \pm(5\times10^{-13}\ \text{Hz} + \text{timebase error} \times f)$ (0.001 Hz ≤ f ≤ 1 MHz)
Settling time	<200 ms

Timebase

(+20 °C to +30 °C ambient)

Stability	
Std. timebase	<5 ppm
Opt. 02 (OCXO)	<0.01 ppm
Opt. 03 (Rb)	<0.0001 ppm
Aging	
Std. timebase	<5 ppm/year
Opt. 02 (OCXO)	<0.2 ppm/year
Opt. 03 (Rb)	<0.0005 ppm/year
External input	10 MHz ± 10 ppm, sine >0.5 Vpp, 1 kΩ
Output	10 MHz, 1.41 Vpp sine into 50 Ω

Noise & Spurs

Phase noise (at *622.08 MHz)*	
100 Hz offset	<−80 dBc/Hz
1 kHz offset	<−95 dBc/Hz
10 kHz offset	<−100 dBc/Hz
100 kHz offset	<−105 dBc/Hz
Phase noise vs. freq.	6 dB/oct. relative to 622.08 MHz (f ≥ 1 MHz)
Spurious	
f ≥ 1 MHz	<−70 dBc (within 50 kHz of carrier)
f < 1 MHz	<−60 dBc (within 50 kHz of carrier)

Jitter

Jitter (rms)	
1 mHz ≤ f ≤ 1 kHz	<0.015 % of the period
1 kHz < f ≤ 1 MHz	<0.045 % of the period
1 MHz < f ≤ 2 GHz	<1 ps (1 kHz to 5 MHz bandwidth)

Time Modulation

(f ≥ 1 MHz)

Rear-panel input	BNC, DC coupled, 1 kΩ
Sensitivity	1 ns/V, ±5 %
Range	±5 ns
Bandwidth	DC to greater than 10 kHz

Phase setting

Range	±999,999.999°
Resolution	0.001°
Maximum step size	±360° (less for negative steps <4 Hz)
Slew time	<300 ms

Q and $\overline{Q}$ Outputs

Outputs	Front-panel BNC connectors
Frequency range	0.001 Hz to 2.05 GHz
High level	$-2.00\ \text{V} \le V_{HIGH} \le +5.00\ \text{V}$
Amplitude	$200\ \text{mV} \le V_{AMPL} \le 1.00\ \text{V}$ ($V_{AMPL} \equiv V_{HIGH} - V_{LOW}$)
Level resolution	10 mV
Level error	<1 % + 10 mV
Transition time	<300 ps (20 % to 80 %)
Symmetry (f > 1 MHz)	<±100 ps departure from nominal 50 %
Source impedance	50 Ω (±1 %)
Load impedance	50 Ω to ground on both outputs
Pre-programmed levels	+5.0 V PECL to +3.3 V PECL, LVDS, +7 dBm, ECL
Protection	Continuous to ground, momentary to ±5 V

CMOS Output

Output	Front-panel BNC
Frequency range	0.001 Hz to 250 MHz
Low level	$-1.00\ \text{V} \le V_{LOW} \le +1.00\ \text{V}$
Amplitude	$500\ \text{mV} \le V_{AMPL} \le 6.00\ \text{V}$ ($V_{AMPL} \equiv V_{HIGH} - V_{LOW}$)
Level resolution	10 mV
Level error	<1 % + 10 mV
Transition time	<1 ns (20 % to 80 %)
Symmetry (f > 1 MHz)	<±500 ps departure from nominal 50 %
Source impedance	50 Ω (reverse terminates cable reflection)
Load impedance	Unterminated 50 Ω cable of any length
Attenuation (50 Ω load)	Output levels are divided by 2
Pre-programmed levels	$V_{LOW} = 0$ $V_{HIGH} = 1.2$, 1.8, 2.5, 3.3, or 5.0 V
Protection	Continuous to ground, momentary to ±5 V

RS-485 Output

Output	Rear-panel RJ-45
Frequency range	0.001 Hz to 50 MHz
Clock output	Pin 1 and pin 2 drive twisted pair
Load impedance	100 Ω between pin 7 and pin 8
Logic levels (RS-485)	$V_{LOW} = +1.5$ V, $V_{HIGH} = +3.5$ V
Recommended cable	Straight-through Category-6
Protection	Continuous to ground, momentary to ±5 V

LVDS Output

(EIA/TIA-644)

Output	Rear-panel RJ-45
Frequency range	0.001 Hz to 2.05 GHz
Clock	Pin 1 and pin 2 to drive twisted pair
Source impedance	100 Ω between pin 1 and pin 2
Load impedance	100 Ω between pin 1 and pin 2
Recommended cable	Straight-through Category-6
Protection	Continuous to ground, momentary to ±5 V

PRBS (Opt. 01)

(EIA/TIA-644)

Level	LVDS on rear-panel SMA jacks
Outputs	PRBS, –PRBS, CLK and –CLK
PRBS generator	x^7+x^6+1 for a length of 2^7-1 bits
Transition time (typ.)	80 ps (20 % to 80 %)
Load impedance	50 Ω to ground on all outputs

Accessory Power

(on rear-panel RJ-45 connector)

+5 VDC	Pin 3
–5 VDC	Pin 5
Ground return	Pin 4 and pin 6
Short circuit protection	Current limited to 250 mA
Polarity clamps	Diode clamps prevent polarity inversion
	(2 ADC max., 120 A non-rep.)

General

Computer interfaces	IEEE-488.2 and RS-232 standard.
All	instrument functions can be controlled through the computer interfaces.
Non-volatile memory	Ten sets of instrument configurations can be stored and recalled.
Line power	Universal input, 90 to 264 VAC, 47 Hz to 63 Hz
Standby power	<5 W (std. timebase) <15 W (opt. 02, OCXO timebase) <25 W (opt. 03, Rb timebase)
Operating power	<30 W (std. timebase) <40 W (opt. 02, OCXO timebase) <50 W (opt. 03, Rb timebase)
Dimensions	8.5"×3.5"×13" (WHD)
Weight	9 lbs.
Warranty	One year parts and labor on defects in materials and workmanship

Ordering Information

CG635	Synthesized clock generator
Option 01	PRBS w/ complementary LVDS outputs on SMA
Option 02	OCXO timebase
Option 03	Rubidium timebase
CG640	CMOS (+5 Vcc) to 50 MHz
CG641	CMOS (+3.3 Vcc) to 250 MHz
CG642	CMOS (+2.5 Vcc) to 250 MHz
CG643	PECL (+5 Vcc) to 1500 MHz
CG644	PECL (+3.3 Vcc) to 1500 MHz
CG645	PECL (+2.5 Vcc) to 1500 MHz
CG646	RF (+7 dBm) to 1500 MHz
CG647	CML/NIM to 1500 MHz
CG648	ECL to 1500 MHz
CG649	LVDS to 2050 MHz
CG650	All ten receivers (CG640-CG649)
O635RMD	Double rack mount kit
O635RMS	Single rack mount kit